Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted with the Information Disclosure Statement filed on February 1, 2001, marked as being considered and initialed by the Examiner, be returned with the next official communication.

§103 Rejections of the Claims

Claims 1-52 and 108-154 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the admitted prior art (APA) in view of Yamamoto et al (U.S. 6,265,782) , Penry (US 6,049,094), Satsu et al. (US 6,225,418) and Narita (US 6,144,107). Applicant traverses the rejections of claims 1-52, 108-126 and 136-154. Claims 127-135 are cancelled, so the rejections are moot. Applicant does not admit that the cited references are prior art and reserves the right to "swear behind" each of the cited references as provided for under 37 C.F.R. 1.131.

Applicant objects to the office action alluding to "admitted prior art." Applicant respectfully submits that the office action must clearly state the grounds of the rejection. M.P.E.P. § 707.07(d). Merely alluding to "admitted prior art" does not meet the standard of clearly stating the grounds of the rejection as required by the M.P.E.P. Thus, the rejections are improper. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 1-52 and 108-154.

Claims 1-52 and 108-154 are rejected in view of four references. The office action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002). Since the office action fails to address this issue, the office action fails to support a finding of a suggestion or motivation to combine the teachings of the four references. Hence, the office action fails to meet the standard of *In re Sang Su Lee.* Thus, the office action fails to state a *prima facie* case of obviousness with respect to claims 1-52 and 108-154. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 1-52 and 108-154.

Claims 1 and 108 recite, "a material having a Young's modulus of between about .1 megapascals and about 20 megapascals." In contrast, Yamamoto et al. teaches in the abstract of the patent, "an adhesive having a storage elastic modulus at 25° C, of from 10 to 2,000 MPa and a storage elastic modulus at 260° C. of from 3 to 50 MPa." In addition, the other cited references fail to teach or suggest "a material having a Young's modulus of between about .1 megapascals and about 20 megapascals." Hence, the cited references do not teach or suggest, either alone or in combination, each of the elements recited in claims 1 and 108. Thus, the office action fails to state a *prima facie* case of obviousness with respect to claims 1 and 108.

Claims 2-17 are dependent on claim 1. Claims 109-126 are dependent on claim 108. For reasons analogous to those provided above and the elements in the claims, applicant respectfully submits that the office action fails to state a *prima facie* case of obviousness with respect to claims 2-17 and 109-126.

Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 1-17 and 108-126.

Claims 35 and 136 recite, "a rigid die attach material." The office action fails to recite the word "rigid," and the office action fails to cite to a reference that teaches or suggests "a rigid die attach material." For example, in contrast to claims 35 and 136, Yamamoto et al. teaches at column 18, lines 25-30, "More specifically, the triple-layer structure of the present invention can make it easy to automate operations for registration of the adhesive film having *no rigidity*. . . . [emphasis added]" Hence, the cited references fail to teach or suggest, either alone or in combination, each of the elements recited in claims 35 and 136. (Applicant also notes that Yamamoto et al. teaches away from the claims 35 and 136, and "teaching away" is a factor to be considered in determining whether references include a teaching, suggestion or motivation to combine, which is required to establish a *prima facie* case of obviousness.) Thus, the office action fails to state a *prima facie* case of obviousness with respect to claims 35 and 136.

Claims 36-52 are dependent on claim 35. Claims 137-154 are dependent on claim 136. For reasons analogous to those provided above and the elements in the claims, applicant respectfully submits that the office action fails to state a *prima facie* case of obviousness with respect to claims 36-52 and 137-154.

Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 36-52 and 137-154.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone applicant's attorney at 612- 371-2109 to facilitate prosecution of the application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 5th day of September, 2002.

Name Amy Moriarty Signature Amy Moriarty

Docket No. 303.706US1
WD # 448056

Micron Ref. No. 99-1307

Clean Version of Pending Claims

ELECTRONIC DEVICE PACKAGE
Applicant: Tongbi Jiang et al.
Serial No.: 09/775,366

Claims 1-52, 108-126, 136-154, and 252-269, as of September 5, 2002 (date response to first office action filed).

1. An integrated circuit package comprising:

a substrate;

a die; and

a material having a Young's modulus of between about .1 megapascals and about 20 megapascals, at a solder reflow temperature, attaching the die to the substrate.

2. The integrated circuit package of claim 1, wherein the substrate comprises a ceramic.

3. The integrated circuit package of claim 1, wherein the die comprises one or more memory circuits.

4. The integrated circuit package of claim 1, wherein the die comprises one or more processor circuits.

5. The integrated circuit package of claim 1, wherein the die comprises one or more logic circuits.

6. The integrated circuit package of claim 1 wherein the die comprises one or more application specific integrated circuits.

7. The integrated circuit package of claim 1, wherein the material comprises a poly epoxide formed from one epoxide.

8. The integrated circuit package of claim 1, wherein the material comprises a poly epoxide formed from two or more epoxides.

9. The integrated circuit package of claim 1, wherein the material comprises a polyacrylate.

10. The integrated circuit package of claim 1, wherein the material comprises a polyolefin.

11. The integrated circuit package of claim 1, wherein the material comprises a polyimide.

12. The integrated circuit package of claim 1, wherein the material comprises a mixture of at least two of a poly epoxide, polyacrylate, polyimide, and polyolefin.

13. The integrated circuit package of claim 1, wherein the material comprises a copolymer of at least two of a poly epoxide, a polyacrylate, polyimide, and polyolefin.

14. The integrated circuit package of claim 1, wherein the material comprises a mixture of a poly epoxide and a polyimide.

15. The integrated circuit package of claim 1, wherein the material comprises a copolymer of a poly epoxide and a polyimide.

16. The integrated circuit package of claim 1, wherein the material has a Shore A hardness of greater than about 70.

17. The integrated circuit package of claim 1, wherein the material has a Shore D hardness of greater than about 20.

18. An integrated circuit package comprising:

a substrate;

a die; and

a material having a coefficient of thermal expansion α_2 of less than about 400 (four-hundred) ppm/°C attaching the die to the substrate.

19. The integrated circuit package of claim 18, wherein the substrate comprises a single metal layer glass-epoxide.

20. The integrated circuit package of claim 18, wherein the die comprises one or more processor circuits.

21. The integrated circuit package of claim 18 wherein the die comprises one or more memory circuits.

22. The integrated circuit package of claim 18, wherein the die comprises one or more logic circuits.

23. The integrated circuit package of claim 18, wherein the die comprises one or more application specific integrated circuits.

24. The integrated circuit package of claim 18, wherein the material comprises a poly epoxide formed from one epoxide.

25. The integrated circuit package of claim 18, wherein the material comprises a poly epoxide formed from two or more epoxides.

26. The integrated circuit package of claim 18, wherein the material comprises a polyacrylate.

27. The integrated circuit package of claim 18, wherein the material comprises a polyolefin.

28. The integrated circuit package of claim 18, wherein the material comprises a polyimide.

29. The integrated circuit package of claim 18, wherein the material comprises a mixture of at least two of a poly epoxide, polyacrylate, polyimide, and polyolefin.

30. The integrated circuit package of claim 18, wherein the material comprises a copolymer of at least two of a poly epoxide, a polyacrylate, polyimide, and polyolefin.

31. The integrated circuit package of claim 18, wherein the material comprises a mixture of a poly epoxide and a polyimide.

32. The integrated circuit package of claim 18, wherein the material comprises a copolymer of a poly epoxide and a polyimide.

33. The integrated circuit package of claim 18, wherein the material has a Shore A hardness of greater than about 70.

34. The integrated circuit package of claim 18, wherein the material has a Shore D hardness of greater than about 20.

35. An integrated circuit package comprising:

a substrate;

a die; and

a rigid die attach material attaching the die to the substrate.

36. The integrated circuit package of claim 35, wherein the substrate comprises a printed circuit board.

37. The integrated circuit package of claim 35, wherein the die comprises a communication circuit.

38. The integrated circuit package of claim 35, wherein the die comprises one or more memory circuits.

39. The integrated circuit package of claim 35, wherein the die comprises one or more processor circuits.

40. The integrated circuit package of claim 35, wherein the die comprises one or more logic circuits.

41. The integrated circuit package of claim 35, wherein the die comprises one or more application specific integrated circuits.

42. The integrated circuit package of claim 35, wherein the rigid die attach material comprises a poly epoxide formed from one epoxide.

43. The integrated circuit package of claim 35, wherein the rigid die attach material comprises a poly epoxide formed from two or more epoxides.

44. The integrated circuit package of claim 35, wherein the rigid die attach material comprises a polyacrylate.

45. The integrated circuit package of claim 35, wherein the rigid die attach material comprises a polyolefin.

46. The integrated circuit package of claim 35, wherein the rigid die attach material comprises a polyimide.

47. The integrated circuit package of claim 35, wherein the rigid die attach material comprises a mixture of at least two of a poly epoxide, polyacrylate, polyimide, and polyolefin.

48. The integrated circuit package of claim 35, wherein the rigid die attach material comprises a copolymer of at least two of a poly epoxide, a polyacrylate, polyimide, and polyolefin.

49. The integrated circuit package of claim 35, wherein the rigid die attach material comprises a mixture of a poly epoxide and a polyimide.

50. The integrated circuit package of claim 35, wherein the rigid die attach material comprises a copolymer of a poly epoxide and a polyimide.

51. The integrated circuit package of claim 35, wherein the rigid die attach material has a Shore A hardness of greater than about 70.

52. The integrated circuit package of claim 35, wherein the rigid die attach material has a Shore D hardness of greater than about 20.

108. An integrated circuit package comprising:

a ceramic substrate;

a die; and

a material having a Young's modulus of between about .1 and about 20, at a solder reflow temperature, attaching the die to the substrate.

109. The integrated circuit package of claim 108, wherein the ceramic substrate comprises a multi-metal layer ceramic substrate.

110. The integrated circuit package of claim 108, wherein the die comprises a communication circuit fabricated on a semiconductor.

111. The integrated circuit package of claim 108, wherein the die comprises one or more memory circuits.

112. The integrated circuit package of claim 108, wherein the die comprises one or more processor circuits.

113. The integrated circuit package of claim 108, wherein the die comprises one or more logic circuits.

114. The integrated circuit package of claim 108, wherein the die comprises one or more application specific integrated circuits.

115. The integrated circuit package of claim 108, wherein the material comprises one or more epoxides, poly epoxides, copolymers of epoxides, or mixtures thereof.

116. The integrated circuit package of claim 108, wherein the material comprises a poly epoxide formed from one epoxide.

117. The integrated circuit package of claim 108, wherein the material comprises a poly epoxide formed from two or more epoxides.

118. The integrated circuit package of claim 108, wherein the material comprises a polyacrylate.

119. The integrated circuit package of claim 108, wherein the material comprises a polyolefin.

120. The integrated circuit package of claim 108, wherein the material comprises a polyimide.

121. The integrated circuit package of claim 108, wherein the material comprises a mixture of at least two of a poly epoxide, polyacrylate, polyimide, and polyolefin.

122. The integrated circuit package of claim 108, wherein the material comprises a copolymer of at least two of a poly epoxide, a polyacrylate, polyimide, and polyolefin.

123. The integrated circuit package of claim 108, wherein the material comprises a mixture of a poly epoxide and a polyimide.

124. The integrated circuit package of claim 108, wherein the material comprises a copolymer of a poly epoxide and a polyimide.

125. The integrated circuit package of claim 108, wherein the material has a Shore A hardness of greater than about 70.

126. The integrated circuit package of claim 108, wherein the material has a Shore D hardness of greater than about 20.

136. An integrated circuit package comprising:
a ceramic substrate;
a die; and
a rigid die attach material attaching the die to the substrate.

137. The integrated circuit package of claim 136, wherein the ceramic substrate comprises a multilayered ceramic substrate.

138. The integrated circuit package of claim 136, wherein the die comprises germanium.

139. The integrated circuit package of claim 136, wherein the die comprises one or more memory circuits.

140. The integrated circuit package of claim 136, wherein the die comprises one or more processor circuits.

141. The integrated circuit package of claim 136, wherein the die comprises one or more logic circuits.

142. The integrated circuit package of claim 136, wherein the die comprises one or more application specific integrated circuits.

143. The integrated circuit package of claim 136, wherein the rigid die attach material comprises one or more epoxides, poly epoxides, copolymers of epoxides, or mixtures thereof.

144. The integrated circuit package of claim 136, wherein the rigid die attach material comprises a poly epoxide formed from one epoxide.

145. The integrated circuit package of claim 136, wherein the rigid die attach material comprises a poly epoxide formed from two or more epoxides.

146. The integrated circuit package of claim 136, wherein the rigid die attach material comprises a polyacrylate.

147. The integrated circuit package of claim 136, wherein the rigid die attach material comprises a polyolefin.

148. The integrated circuit package of claim 136, wherein the rigid die attach material comprises a polyimide.

149. The integrated circuit package of claim 136, wherein the rigid die attach material comprises a mixture of at least two of a poly epoxide, polyacrylate, polyimide, and polyolefin.

150. The integrated circuit package of claim 136, wherein the rigid die attach material comprises a copolymer of at least two of a poly epoxide, a polyacrylate, polyimide, and polyolefin.

151. The integrated circuit package of claim 136, wherein the rigid die attach material comprises a mixture of a poly epoxide and a polyimide.

152. The integrated circuit package of claim 136, wherein the rigid die attach material comprises a copolymer of a poly epoxide and a polyimide.

153. The integrated circuit package of claim 136, wherein the rigid die attach material has a Shore A hardness of greater than about 70.

154. The integrated circuit package of claim 136, wherein the rigid die attach material has a Shore D hardness of greater than about 20.

252. An integrated circuit package comprising:

a substrate;

a die; and

a material having a coefficient of thermal expansion α_2 of between about one and about sixty-two ppm/°C attaching the die to the substrate.

253. The integrated circuit package of claim 252, wherein the substrate comprises a single metal layer glass-epoxide.

254. The integrated circuit package of claim 252, wherein the die comprises one or more processor circuits.

255. The integrated circuit package of claim 252 wherein the die comprises one or more memory circuits.

256. The integrated circuit package of claim 252, wherein the die comprises one or more logic circuits.

257. The integrated circuit package of claim 252, wherein the die comprises one or more application specific integrated circuits.

258. The integrated circuit package of claim 252, wherein the material comprises a poly epoxide formed from one epoxide.

259. The integrated circuit package of claim 252, wherein the material comprises a poly epoxide formed from two or more epoxides.

260. The integrated circuit package of claim 252, wherein the material comprises a polyacrylate.

261. An integrated circuit package comprising:

a substrate;

a die; and

a material having a coefficient of thermal expansion α_2 of between about 151 (one-hundred and fifty-one) and about 400 (four-hundred)] ppm/°C attaching the die to the substrate.

262. The integrated circuit package of claim 261, wherein the material comprises a polyolefin.

263. The integrated circuit package of claim 261, wherein the material comprises a polyimide.

264. The integrated circuit package of claim 261, wherein the material comprises a mixture of at least two of a poly epoxide, polyacrylate, polyimide, and polyolefin.

265. The integrated circuit package of claim 261, wherein the material comprises a copolymer of at least two of a poly epoxide, a polyacrylate, polyimide, and polyolefin.

266. The integrated circuit package of claim 261, wherein the material comprises a mixture of a poly epoxide and a polyimide.

267. The integrated circuit package of claim 261, wherein the material comprises a copolymer of a poly epoxide and a polyimide.

268. The integrated circuit package of claim 261, wherein the material has a Shore A hardness of greater than about 70.

269. The integrated circuit package of claim 261, wherein the material has a Shore D hardness of greater than about 20.